WHAT IS CLAIMED IS

1. An apparatus for delaying a digital signal for a predetermined delay period of time, the digital signal having a first and a second logic levels, comprising:

a first edge detection circuit which detects a first edge of the digital signal whereon the level of the digital signal changes from the first logic level to the second logic level, and generates a first detection signal;

a set circuit which includes a first counter for counting a reference clock signal to generate a count value and clearing its own count value in response to the first detection signal, wherein the set circuit generates a set signal if the count value reaches the number of the reference clock signals corresponding to the delay period of time;

a reset circuit which generates a reset signal if an elapsed period of time since a generation of the set signal equals to a period of time while the digital signal maintain the second logic level; and

an output circuit which outputs a digital signal including edges synchronized with the set signal and the reset signal.

2. The apparatus of claim 1, wherein the reset circuit comprises:

a first storage circuit which stores the number of reference clock signals corresponding to the period of time while the digital signal maintain the second logic level; and

a first comparator which compares the count value of the

first counter with a total value added the number of the references clock signal corresponding to the delay period of time to the number of reference clock signals corresponding to the period of time while the digital signal maintain the second logic level, and generates the reset signal if the count value of the first counter equals to the total value.

3. The apparatus of claim 1, wherein the apparatus further comprises:

a second edge detection circuit which detects a second edge of the digital signal whereon the level of the digital signal changes from the second logic level to the first logic level, and generates a second detection signal;

and wherein the reset circuit comprises:

a second storage circuit which stores the count value of the first counter in response to the second edge detection signal;

a second counter which counts the reference clock signal to generate a count value and clears its own count value in response to the set signal; and

a second comparator which compares the count value of the second counter with the count value stored by the second storage circuit, and generates the reset signal if the count value of the second counter equals to the count value stored by the second storage circuit.

4. The apparatus of claim 1, wherein the apparatus further comprises:

a second edge detection circuit which detects a second

edge of the digital signal whereon the level of the digital signal changes from the second logic level to the first logic level, and generates a second detection signal;

and wherein the reset circuit comprises:

a third counter which counts the reference clock signal to generate a count value and clears its own count value in response to the second detection signal; and

a third comparator which compares the count value of the third counter with the number of the reference clock signals corresponding to the delay period of time, and generates the reset signal if the count value of the third counter equals to the number of the reference clock signals corresponding to the delay period of time.

5. An apparatus for delaying a digital signal for a predetermined delay period of time, the digital signal having a first and a second logic levels, comprising:

a third edge detection circuit which detects a first edge of the digital signal and a second edge of the digital signal, wherein on the first edge the level of the digital signal changes from the first logic level to the second logic level, wherein on the second edge the level of the digital signal changes from the second logic level to the first logic level, and generates a third detection signal;

an write address counter which changes an write address value in response to the third edge detection signal, and clears its own write address value in response to a system reset signal;

an write counter which counts a reference clock signal to generate an write count value, and resets its own write count

value at a first initial value in response to the system reset signal;

a third storage circuit which stores the write count value, wherein the write count value is written into the third storage circuit in accordance with the write address value and read out from the third storage circuit in accordance with the read address value;

a read counter which counts the reference clock signal to generate a read count value, and resets its own read count value at a second initial value in response to the system reset signal, wherein the second initial value has a difference of a value added one to the number of the reference clock signals corresponding to the delay period of time between the first initial value;

a fourth comparator which compares the read count value with the write count value read out from the third storage circuit, and generates a detection signal if the read count value equals to the write count value read out from the third storage circuit;

a read address counter which changes the read address value in response to the detection signal of the fourth comparator, and clears its own read address value in response to a system reset signal; and

an output circuit which outputs the least significant bit of the read address value.

6. The apparatus of claim 5, wherein the apparatus further comprises:

a judgment circuit which judges whether the delay period

of time is set or not based on the second initial value;

and wherein the output circuit outputs the least significant bit of the write address value if the delay period of time is not set.

7. A method for delaying a digital signal for a predetermined delay period of time, the digital signal having a first and a second logic levels, comprising the steps of:

(A) detecting a first edge of the digital signal whereon the level of the digital signal changes from the first logic level to the second logic level, and generating a first detection signal;

(B) counting a reference clock signal to output a count value and clearing its own count value in response to the first detection signal, and generating a set signal if the count value reaches the number of the reference clock signals corresponding to the delay period of time;

(C) generating a reset signal if an elapsed period of time since a generation of the set signal equals to a period of time while the digital signal maintain the second logic level; and

(D) outputting a pulse signal including edges synchronized with the set signal and the reset signal.

8. The method of claim 7, wherein the step (C) comprises the substeps of:

(c1) storing the number of reference clock signals corresponding to the period of time while the digital signal maintain the second logic level; and

(c2) comparing the count value of counted in the step (B) with a total value added the number of the reference clock signals corresponding to the delay period of time to the number of reference clock signals corresponding to the period of time while the digital signal maintain the second logic level, and generating the reset signal if the count value counted in the step (B) equals to the total value.

9. The method of claim 7, wherein the method further comprises the step of:

(E) detecting a second edge of the digital signal whereon the level of the digital signal changes from the second logic level to the first logic level, and generating a second detection signal;

and wherein the step (C) comprises the substeps of:

(c3) storing the count value counted in the step (B) in response to the second edge detection signal;

(c4) counting the reference clock signals to generate a count value and clearing its own count value in response to the set signal; and

(c5) comparing the count value counted in the substep (c4) with the stored count value, and generating the reset signal if the count value counted in the substep (c4) equals to the stored count value.

10. The method apparatus of claim 7, wherein the method further comprises the step of:

(F) detecting a second edge of the digital signal whereon the level of the digital signal changes from the second logic

level to the first logic level, and generating a second detection signal;

and wherein the step (C) comprises the substeps of:

(c6) counting the reference clock signal to generate a count value and clearing its own count value in response to the second detection signal; and

(c7) comparing the count value counted in the substep (c6) with the number of the reference clock signals corresponding to the delay period of time, and generating the reset signal if the count value counted in the substep (c6) equals to the number of the reference clock signals corresponding to the delay period of time.

11. A method for delaying a digital signal for a predetermined delay period of time, the digital signal having a first and a second logic levels, comprising the steps of:

(G) detecting a first edge of the digital signal and a second edge of the digital signal, wherein on the first edge the level of the digital signal changes from the first logic level to the second logic level, wherein on the second edge the level of the digital signal changes from the second logic level to the first logic level, and generating a third detection signal;

(H) changing an write address value in response to the third edge detection signal, and clearing its own write address value in response to a system reset signal;

(I) counting a reference clock signal to output an write count value, and resetting the write count value at a first initial value in response to the system reset signal;

(J) storing the write count value, wherein the write count value is written into the third storage circuit in accordance with the write address value and read out from the third storage circuit in accordance with the read address value ;

(K) counting the reference clock signal to output a read count value, and resetting the read count value at a second initial value in response to the system reset signal, wherein the second initial value has a difference of a value added one to the number of the reference clock signals corresponding to the delay period of time between the first initial value;

(L) comparing the read count value with the write count value read out in the step (J), and generating a detection signal if the read count value equals to the write count value read out in the step (J);

(M) changing the read address value in response to the detection signal, and clearing its own read address value in response to a system reset signal; and

(N) outputting the least significant bit of the read address value.

12. The method of claim 11, wherein the method further comprises the steps of:

(O) judging whether the delay period of time is set or not based on the second initial value;

and wherein the step (N) outputting the least significant bit of the write address value if the delay period of time is not set.

13. An apparatus for delaying a digital signal for a

predetermined delay period of time, the digital signal having a first and a second logic levels, comprising:

a first edge detection means for detecting a first edge of the digital signal whereon the level of the digital signal changes from the first logic level to the second logic level, and generating a first detection signal;

a set means, which includes a first counter for counting a reference clock signal to generate a count value and clearing its own count value in response to the first detection signal, wherein the set means for generating a set signal if the count value reaches the number of the reference clock signals corresponding to the delay period of time;

a reset means for generating a reset signal if an elapsed period of time since a generation of the set signal equals to a period of time while the digital signal maintain the second logic level; and

an output means for outputting a pulse signal including edges synchronized with the set signal and the reset signal.

14. The apparatus of claim 13, wherein the reset means comprises:

a first storage means for storing the number of reference clock signals corresponding to the period of time while the digital signal maintain the second logic level; and

a first comparing means for comparing the count value of the first counter with a total value added the number of the references clock signal corresponding to the delay period of time to the number of reference clock signals corresponding to the period of time while the digital signal maintain the second

logic level, and generating the reset signal if the count value of the first counter equals to the total value.

15. The apparatus of claim 13, wherein the apparatus further comprises:

a second edge detection means for detecting a second edge of the digital signal whereon the level of the digital signal changes from the second logic level to the first logic level, and generating a second detection signal;

and wherein the reset means comprises:

a second storage means for storing the count value of the first counter in response to the second edge detection signal;

a second counter which counts the reference clock signal to generate a count value and clearing its own count value in response to the set signal; and

a second comparing means for comparing the count value of the second counter with the count value stored by the second storage means, and generating the reset signal if the count value of the second counter equals to the count value stored by the second storage means.

16. The apparatus of claim 13, wherein the apparatus further comprises:

a second edge detection means for detecting a second edge of the digital signal whereon the level of the digital signal changes from the second logic level to the first logic level, and generating a second detection signal;

and wherein the reset means comprises:

a third counter which counts the reference clock signal to generate a count value and clearing its own count value in response to the second detection signal; and

a third comparing means for comparing the count value of the third counter with the number of the reference clock signals corresponding to the delay period of time, and generating the reset signal if the count value of the third counter equals to the number of the reference clock signals corresponding to the delay period of time.

17. An apparatus for delaying a digital signal for a predetermined delay period of time, the digital signal having a first and a second logic levels, comprising:

a third edge detection means for detecting a first edge of the digital signal and a second edge of the digital signal, wherein on the first edge the level of the digital signal changes from the first logic level to the second logic level, wherein on the second edge the level of the digital signal changes from the second logic level to the first logic level, and generating a third detection signal;

an write address count means for changing an write address value in response to the third edge detection signal, and clearing its own write address value in response to a system reset signal;

an write count means for counting a reference clock signal to generate an write count value, and resetting its own write count value at a first initial value in response to the system reset signal;

a third storage means for storing the write count value,

wherein the write count value is written into the third storage circuit in accordance with the write address value and read out from the third storage circuit in accordance with the read address value;

a read count means for counting the reference clock signal to generate a read count value, and resetting its own read count value at a second initial value in response to the system reset signal, wherein the second initial value has a difference of a value added one to the number of the reference clock signals corresponding to the delay period of time between the first initial value;

a fourth comparing means for comparing the read count value with the write count value read out from the third storage means, and generating a detection signal if the read count value equals to the write count value read out from the third storage means;

a read address count means for changing the read address value in response to the detection signal, and clearing its own read address value in response to a system reset signal; and

an output means for outputting the least significant bit of the read address value.

18. The apparatus of claim 17, wherein the apparatus further comprises:

a judgment means for judging whether the delay period of time is set or not based on the second initial value;

and wherein the output means for outputting the least significant bit of the write address value if the delay period of time is not set.